CMOS CURRENT MODE RF DETECTOR AND METHOD

Background of the Invention

[0001] The present invention relates in general to semiconductor devices and, more particularly, to high frequency detector circuits.

[0002] In most if not all countries, the transmission of high frequency signals is controlled by industry standards and/or by government regulation. For example, transmitted signals in cellular telephones and other wireless communication devices are limited to operating in predefined frequency bands ranging from about four hundred megahertz to about 2.5 gigahertz. The amplitudes of the transmitted signals also are limited to avoid interference with other devices operating in the same or adjacent frequency bands. In addition, manufacturers extend the battery life of the wireless devices by reducing the transmitted power when such a reduction is possible without interrupting communications.

[0003] In order to control the transmitted power, a high frequency signal typically is monitored with a radio frequency (RF) detector that senses the signal's amplitude and produces a corresponding detection signal. A control circuit uses the detection signal and other communications information to control a power amplifier that produces the transmitted signal at an appropriate amplitude.

[0004] Previous systems use discrete devices such as Schottky diodes for the RF detectors. However, the discrete devices require additional circuitry to generate a useful detection signal, which increases the system's parts count as well as its size and manufacturing cost. Other systems integrate the Schottky diodes with the control circuitry to form a single integrated circuit. However, this scheme increases the complexity of the fabrication process, which

increases the fabrication cost of the integrated circuit and can reduce the die yield, further increasing the cost.

[0005] Hence, there is a need for an integrated RF detector circuit and detection method that reduces the physical size and manufacturing cost of a wireless communications system.

Brief Description of the Drawings

[0006] FIG. 1 is a block diagram of a power stage of a wireless communications device; and

FIG. 2 is a schematic diagram of a radio frequency signal detection circuit.

Detailed Description of the Drawings

[0007] In the figures, elements having the same reference number have similar functionality.

[0008] FIG. 1 is a block diagram of a power stage 10 of a wireless communications device such as a cellular telephone, including a microprocessor 11, a control circuit 13, a power amplifier 18 and a coupler 25. Power stage 10 generates a high frequency signal V_{RF} with a carrier frequency component operating at a radio frequency (RF) of about nine hundred megahertz. Other embodiments operate with a high frequency signal V_{RF} that ranges between about four hundred megahertz and about 2.5 gigahertz.

[0009] Microprocessor 11 is a digital processing circuit that includes a digital to analog converter for converting internal digital data to an analog amplitude control signal V_{MAG} to set the magnitude of high frequency signal V_{RF}.

[0010] Power amplifier 18 has a signal input 23 that receives an RF signal V_{RFIN} at a carrier frequency of about nine hundred megahertz that is modulated with analog and/or digital information. Power amplifier 18 amplifies V_{RFIN} to

produce high frequency signal V_{RF} at a node 24 with a power level that can range over about five decades, or an equivalent voltage range from about twenty millivolts to about four volts. An analog amplitude control signal V_{CTRL} is produced at a node 17 by control circuit 13 to control the gain of power amplifier 18 and therefore the amplitude of high frequency signal V_{RF}.

[0011] Coupler 25 is an attenuator that transfers high frequency signal V_{RF} to a transmission line on a node 19 to produce a high frequency signal V_{RFDET} at a reduced amplitude. In one embodiment, coupler 25 attenuates V_{RF} by a factor of ten in order to avoid driving control circuit 13 into an overload condition when V_{RF} has a high amplitude level.

[0012] Control circuit 13 includes a transconductance amplifier 14, a differential transimpedance amplifier 16 and an RF detector 20. Control circuit 13 is formed on a semiconductor die as an integrated circuit fabricated with a standard complementary metal-oxide-semiconductor (CMOS) process using 0.6 micrometer lithography.

[0013] Transconductance amplifier 14 amplifies and converts amplitude control signal V_{MAG} to a proportional current I_{REF} that is provided on a node 15 to function as a reference current.

[0014] RF detector 20 has a sense input on node 19 for detecting or sensing the amplitude of high frequency signal V_{RFDET} to produce a direct current (DC) detection current I_{DET} at an output coupled to a node 21.

[0015] Differential transimpedance amplifier 16 amplifies I_{DET} using current I_{REF} as a reference and produces V_{CTRL} at node 17.

[0016] RF detector 20 is formed with nonlinear elements which are needed to produce DC components of detection current I_{DET} to provide the detection function. RF detector

20 compensates for the nonlinear elements to produce detection current I_{DET} as a substantially linear function of the amplitude of V_{RFDET} as described in detail below.

[0017] FIG. 2 is a schematic diagram showing RF detector 20 in further detail, including a series of parallel-connected transconductance gain stages GS_1, GS_2 . . . GS_N, where N is an integer. In one embodiment, N=5. To prevent standing waves on node 19, a termination resistor 71 is used to match the characteristic impedance of the transmission line designated as node 19. In one embodiment, resistor 71 has a value of about fifty ohms. V_{RFDET} is coupled through a coupling capacitor 80 to a node 82. In one embodiment, coupling capacitor 80 has a value of about ten picofarads. A DC bias voltage V_{BIAS} is coupled through a resistor 72 to provide a DC bias on node 82. Resistor 72 typically has a value at least ten times that of resistor 71 to avoid loading node 19 and attenuating high frequency signal V_{RFDET}.

[0018] Gain stage GS_1 includes a p-channel metal-oxide-semiconductor field effect transistor (MOSFET) PF_1 and an n-channel MOSFET NF_1 configured as shown. The other gain stages are similarly configured so, for example, gain stage GS_2 includes a p-channel MOSFET PF_2 and an n-channel MOSFET NF_2, gain stage GS_N includes a p-channel MOSFET PF_N and an n-channel MOSFET NF_N, and so forth.

[0019] A diode coupled p-channel transistor 79 receives a reference current I_{REF2} from a current source 78 to provide a gate bias potential that establishes maximum currents I_{MAX1} through I_{MAXN} that can flow through MOSFETs PF_1-PF_N, respectively. Transistor 79 is scaled or matched with MOSFETS PF_1-PF_N, so maximum currents I_{MAX1} through I_{MAXN} are multiples of I_{REF2}.

[0020] MOSFETs NF_1-NF_N respectively have first conduction electrodes or sources coupled to a common node 60 and control electrodes or gates coupled to node 82 to receive

bias voltage V_{BIAS}. The effective sizes or widths W_1-W_N of MOSFETs NF_1-NF_N are scaled in predefined ratios and since NF_1-NF_N have the same gate to source potential, quiescent currents $I0_1$-$I0_N$ flow through MOSFETs NF_1-NF_N to common node 60 in the same ratios.

[0021] Common node 60 is maintained at a substantially constant potential by a regulation circuit that includes transistors 73 and 76, a current source 74 and an amplifier 75. Transistor 73 is scaled to MOSFETs NF_1-NF_N and also has its gate receiving bias voltage V_{BIAS}. Current source 74 supplies a reference current I_{REF1} that is scaled to reference current I_{REF2} to establish a reference potential V_{REF1} at an inverting input of amplifier 75. A feedback path from the gate of transistor 76 to common node 60 and the non-inverting input of amplifier 75 maintains the potential of common node 60 substantially constant. As a result, quiescent currents $I0_1$-$I0_N$ have controllable values which are scaled to reference current I_{REF1}.

[0022] In addition to quiescent currents $I0_1$-$I0_N$, MOSFETs NF_1-NF_N produce detection currents IS_1-IS_N, respectively, in response to high frequency signal V_{RFDET}. Quiescent currents $I0_1$-$I0_N$ and detection currents IS_1-IS_N are summed on node 60, routed through a transistor 76 and mirrored in a transistor 77 to produce detection current I_{DET} at node 21 as an output current of RF detector 20.

[0023] Recall that MOSFETs PF_1-PF_N are scaled or ratioed to provide limiting or maximum currents that can flow in gain stages GS_1-GS_N. MOSFETS NF_1-NF_N are also scaled or ratioed to produce quiescent currents $I0_1$-$I0_N$ that establish the operating points of gain stages GS_1-GS_N. The effect of this scaling is to define amplitude breakpoints of high frequency signal V_{RFDET} at which detection currents IS_1-IS_N reach their respective maximum current levels I_{MAX1}-I_{MAXN}. Table I below shows the effective width W_X of MOSFET NF_X,

quiescent currents $I0_X$ through gain stage GS_X, the effective width WP_X of MOSFET PF_X, maximum current I_{MAXX} and the voltage amplitude of high frequency signal V_{RFDET} at which $(I0_X+IS_X)=I_{MAXX}$ for values of X from 1-N in a standard 0.6 micrometer CMOS embodiment in which N=5.

Gain Stage	W_X (um)	I_{MAXX} (A)	$I0_X$	V_{RFDET} when $I_{MAXX}=I0_X+IS_X$	WP_X
GS_1	350 um	35 uA	30 uA	40 mV	37 um
GS_2	78 um	11.5 uA	6.7uA	110 mV	11.5 um
GS_3	45 um	19 uA	3.85uA	320 mV	19 um
GS_4	17 um	43 uA	1.45uA	890 mV	43 um
GS_5	7 um	120uA	0.6uA	2500 mV	120u

Table I.

[0024] The operation of gain stage GS_1 proceeds as follows. MOSFET NF_1 routes a portion of bias current I_{MAX1} to common node 60 as detection current IS_1 in response to high frequency signal V_{RFDET}. When V_{RFDET} reaches an amplitude of about forty millivolts, $IS_1=(I_{MAX1}-I0_1)$ and does not increase with further increases in V_{RFDET}. Gain stages GS_2-GS_5 have similar operation, but their detection currents reach maximum values at different breakpoints as shown in Table I.

[0025] The transfer functions of gain stages GS_1-GS_N are nonlinear over the full amplitude range of V_{RFDET} from zero to about four volts, which is necessary for producing detection currents IS_1-IS_N with DC current components. For example, gain stage GS_1 produced IS_1 as a function of V_{RFDET} in accordance with a transconductance gm_1 given by $gm_1=(IS_1/V_{RFDET})=k*W_1*V_{RFDET}$, approximately, where K is a constant and W_1 is the effective width of MOSFET NF_1. Note that transconductance gm_1 is proportional to W_1, which is a

constant, and to V_{RFDET}, which is a variable. Since gm_1 increases with the amplitude of V_{RFDET}, IS_1 is a nonlinear function of V_{RFDET}. Gain stages GS_2-GS_N have similar transfer functions.

[0026] The detailed operation of RF detector 20 is described as follows when N=5. When the amplitude of V_{RFDET} is less than about forty millivolts, the overall transfer function of RF detector 20 is $I_{DET}=k*(W_1+W_2+W_3+W_4+W_5)*V_{RFDET}^2$, approximately, where W_1-W_5 are the respective widths of MOSFETs NF_1 through NF_5. When high frequency signal V_{RFDET} reaches an amplitude of about forty millivolts, detection current IS_1 reaches its maximum value of (I_{MAX1}-$I0_1$), and further increases in amplitude do not result in further increases in IS_1. Hence, in a range above about forty millivolts, gain stage GS_1 makes no further contribution to I_{DET}. From forty to about one hundred ten millivolts, only gain stages GS_2-GS_5 contribute to the total transconductance of RF detector 20, so $I_{DET}=k*(W_2+W_3+W_4+W_5)*V_{RFDET}^2$, approximately. In a similar fashion, as other V_{RFDET} breakpoints listed in Table I are reached, successive detection currents IS_2-IS_4 reach their maximum levels (I_{MAX2}-I02), . . ., (I_{MAX4}-$I0_4$) to reduce the effective overall transconductance of RF detector 20 in successive steps until V_{RFDET} reaches eight hundred ninety millivolts. At higher V_{RFDET} amplitudes, only gain stage GS_5 contributes to further increases in I_{DET}. In effect, as the nonlinearity of each stage's transconductance increases, RF detector 20 compensates by successively reducing the number of stages that actively contribute to the overall transconductance. The result is a linear transfer function in which I_{DET} is proportional to V_{RFDET}. It is evident that the number of gain stages and/or the breakpoint amplitudes may vary depending on the linearity desired in the overall transfer

function, the degree of nonlinearity of each gain stage and other factors.

[0027] Hence, the present invention provides an integrated circuit operating as an RF detector that has a first gain stage whose input monitors a high frequency signal and routes a first detection current to a node. A second gain stage includes a first current source that supplies a bias current indicative of a predefined amplitude of the high frequency signal. An input of the second gain stage monitors the high frequency signal to route a portion of the bias current to the node as a second detection current. The second detection current is limited to the bias current when the high frequency signal is greater than the predefined amplitude to compensate for a nonlinearity in a transconductance of the second gain stage. Hence, above the predefined amplitude of the high frequency signal, the detector circuit's overall transconductance is modified to compensate for the nonlinearity. Other gain stages operate in a similar fashion to successively apply different transconductances to different amplitude ranges of the high frequency signal, allowing the detector circuit to compensate for nonlinearities in the transconductances of the other gain stages. The result is a substantially linear transfer function in which the overall detection current is proportional to the high frequency signal. Moreover, the detection function is provided on an integrated circuit using standard CMOS processing and without requiring external Schottky diodes or similar devices.